REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The final Office Action dated September 25, 2006, has been received and its contents carefully reviewed. Applicants appreciate the indication by the Examiner that claims 7-10 and 18-23 are allowed.

Claims 1-6 and 11-17 are rejected the Examiner. With this response claims 1 and 11 have been amended. No new matter has been added. Claims 1-23 remain pending in this application.

In the Office Action, Claims 1-6 and 11-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Related Art (hereinafter "ARA") in view of U.S. Publication No. 2002/0196221 to Morita (hereinafter "Morita") and U.S. Publication No. 2001/0038372 to Morita.

Claim 1 recites a method for driving a liquid crystal display including "wherein reducing the number of bits includes converting an odd source data value into an even source data value having the same number of bits as the odd source data, and then reducing the number of bits of the converted even source data."

In the Office Action, the Examiner acknowledges that ARA does not explicitly teach "where reducing the number of bits includes converting an odd source data value into an even source data value." However, the examiner cites Morita as teaching "converting 8 bits to 5 bits, 6 bits to 4 bits, and 6 bits to 3 bits." Applicants submit that assuming for the sake of argument that the conversion described by the Examiner does suggest "converting an odd source data value into an even source data value," Morita does not teach performing the conversion by "converting an odd source data value into an even source data value having the same number of bits as the odd source data, and then reducing the number of bits of the converted even source data." Applicant further submits that Lee does not cure this deficiency in the teachings of ARA and Morita. Applicants submit that ARA, Morita, and Lee, analyzed in any combination, do not teach at least this quoted combination of features recited in claim 1. Accordingly Applicants submit claim 1 and claims 2-6 are allowable over ARA, Morita, and Lee.

Claim 11 recites an apparatus for driving a liquid crystal display having a combination of features including "a modulator for comparing the reduced-bit source data of a current frame with reduced bit source data of a previous frame to modulate the source data by retrieving a stored preset modulated data in accordance with a result of the comparison, wherein a bit number of the reduced-bit source data of the previous frame is the same as that of the current frame, and a bit number of the preset modulated data is more than that of the reduced-bit source data of each previous frame and current frame, and wherein the modulator replaces all of the bits of the source data with preset modulated data."

In the Office Action, the Examiner acknowledges that ARA does not teach a bit converter for reducing a number of bits of the received source data. The Examiner first cites paragraph [0023] of Morita as teaching "a bit converter for reducing the number of bits of the received source data to generate reduced bit source data." Applicants submit that the cited portion of Morita does not teach or suggest "comparing the reduced-bit source data of a current frame with reduced bit source data of a previous frame by retrieving a stored preset modulated data in accordance with a result of the comparison, wherein a bit number of the reduced-bit source data of the previous frame is the same as that of the current frame" For example, paragraph [0023] and FIGs. 2-4 of Morita disclose that the "bit converter" the uses the reduced bit input data solely "to produce second input gray scale data obtained by delaying the output gray scale data fed by the first table section by one frame." However concerning the input data, Morita discloses retrieving from a table using the unreduced input data which in no case has the same bit size as the delayed data. See Morita, FIG. 1, and FIG. 8-11.

The Examiner additionally cites Lee as teaching "wherein a bit number of the reduced bit source data of a previous frame is the same as that of the current frame, and a bit number of the preset modulated data is more than that of the reduced bit source data of each previous and current frame." In particular, the Examiner cites FIG. 11, and paragraphs [0096]-[0102] of Lee. Further, in the Office Action, the Examiner interprets preset to mean "already known." Applicants note that as shown in FIG. 11 and 12 of Lee, and as described in paragraph [0096]-[0102] cited by the examiner, even assuming there is a teaching of using a reduced the number of bits there is no disclosure of "comparing the reduced-bit source data of a current frame with reduced bit source data of a previous frame to modulate the source

data by retrieving a stored preset modulated data in accordance with a result of the comparison" as recited in claim 11, and further no teaching or suggest related to "wherein a bit number of the reduced-bit source data of the previous frame is the same as that of the current frame" also recited in claim 11. Further, Applicants submit that the "preset data" as interpreted by the Examiner is not "stored preset data" as recited in claim 11 and that Lee does not disclose "retrieving a stored preset modulated data in accordance with a result of the comparison" for at least this reason. Accordingly, Applicants submit that Lee does not cure the deficiencies in the teachings of ARA and Morita. Applicants submit that ARA, Morita, and Lee, analyzed singly or in any combination do not teach or suggest all of the elements of claim 11, and that claim 11 and claims 12-17 depending from claim 11 are each allowable over is allowable over ARA, Morita, and Lee.

Applicants believe the foregoing amendments and remarks place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. *A duplicate copy of this sheet is enclosed.*

Respectfully submitted,

Dated: December 26, 2006 By

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